Amendments to the Drawings

Attached hereto are annotated and replacement sheets showing amendments to Figs. 1, 8, 9, 10, 11A, 12, and 13. The changes are shown as highlighted on the annotated sheets. The amendments to the drawings provide certain labeling and numeric identifiers required by the Examiner, as well as assure corresponding reference numerals used in the drawings and specification.

REMARKS

The specification and Abstract have been amended to correct for spelling and grammatical errors. The amendments to the drawings and specification should now overcome the objections thereto, as the specification and drawings now include correct and corresponding references to numeric identifiers. Fig. 12 has been amended to label the signal line between 180 and 120 as the duty corrected signal 301. This is supported by the specification at page 25, lines 8-13. Fig. 1 was objected to because not all the circuit elements are labeled. While labeling of circuit elements is not required, the amended drawings provide the labeling requested.

Claims 1-8 are active in the application.

The applicant's note with appreciation that claims 4-6 have been identified as being drawn to allowable subject matter. In response, claim 4 has been amended to independent form less the word "constant". Claim 6 has been amended to correct a spelling error.

Claim 1 has been amended to eliminate the modifier "constant" because the modifier is not required to distinguish the invention, and may be misleading in the sense that the current source does not produce a constant current when the input frequency changes. Also, claim 1 was amended to require the additional element of a differential amplifier. This additional element is illustrated in Fig. 13 at indicia 193. Also, the differential amplifier is described in the present specification at page 5, lines 17-25, page 6, lines 1-6, page 25, lines 24-27, and page 28, lines 6-13. No new matter has been added.

Claims 1-3 were rejected under 35 USC 102(b) as being anticipated by US patent 4,438,353 to Sano et al. This rejection is traversed.

The present invention provides a delay locked loop (DLL) circuit that is particularly useful in applications that require analog phase control (as opposed to digital phase control). Analog phase control is desired in many applications such as double data rate DRAMS, since analog phase control can provide timing signals that are not limited to 1.0 or 0.5 cycle units. However, prior art analog phase control DLL circuits are relatively power inefficient. This is because power consumption in prior art circuits is designed to be flat over the operating frequency range.

The present inventors have discovered that power consumption in analog DLL circuits can be reduced. Power consumption is reduced by controlling the current supplied to the DLL differential amplifiers. High frequency operation requires relatively high current, but low frequency operation is adequate with reduced current.

Accordingly, in the present invention, current is supplied to the differential amplifiers at a rate that depends on the frequency of the input signal. A high frequency input signal causes the circuit to increase the current supplied to the differential amplifiers. Power efficiency is thereby increased.

These aspects of the invention are clearly set forth in amended claim 1. Specifically, amended claim 1 requires a differential amplifier receiving current from the current source, and a bias generation means that controls the amount of current supplied to the differential amplifiers according to the frequency of the input signal. These features are unique in a DLL circuit.

In comparison, Sano et al. does not teach a DLL circuit, and does not teach a differential amplifier supplied with current according to a frequency of an input signal.

Sano et al. teach an *I^2L logic circuit*, a logic circuit that is completely different from a *delay locked loop circuit*. A delay locked loop circuit controls the delay and phase of an input signal. Hence, delay locked loop circuits are useful in applications requiring signal synchronization and phase control. The I^2L logic circuits of Sano et al. perform only logic functions. The I^2L logic circuits of Sano et al. cannot perform delay locking or phase control. Sano et al. does not in any way teach or suggest a delay locked loop circuit. There is simply no way to modify a I^2L logic circuit to perform delay locked loop functions. Accordingly, the teachings of Sano et al. fail to meet the limitations of claim 1 requiring a delay locked loop circuit.

Also, Sano et al. do not teach or suggest a differential amplifier, or teach or suggest a differential amplifier controlled with a variable, frequency-dependent current source. An I^2L logic circuit is not a differential amplifier and cannot be modified to function as a differential amplifier. A differential amplifier is wholly absent from Sano et al. Accordingly, Sano et al. does not meet claim 1 as amended.

Claims 7 and 8 were rejected under 35 USC 103(a) as being unpatentable over Sano et al. in view of the admitted prior art. This rejection is traversed.

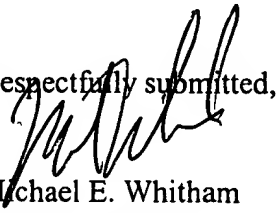
The Office Action presents a theory that it would be obvious to modify Sano's I^2L circuit according to the admitted prior art. This is erroneous because there exists no motivation in Sano et al. or the admitted prior art to add a phase shifter, phase comparator, phase synchronizer and duty correction circuit to an I^2L logic circuit. Sano et al. teach a logic circuit with a variable current supply. Sano et al. does not teach or suggest that a variable current supply can be used with a delay locked loop or any other circuit having a phase shifter, phase comparator, phase synchronizer and/or duty correction circuit. Also, the admitted prior art does not teach or suggest a variable current source in a DLL circuit or an I^2L circuit. The admitted prior art provides no suggestion or motivation to modify an I^2L circuit or any other feature of Sano et al. I^2L logic circuits and delay locked loops circuits are very different in function, application, and design, and so there is simply no motivation to combine features in these two types of circuits. The reasoning in the Office Action appears to be based on impermissible hindsight and a contrived combining together of features.

In view of the foregoing, it is respectfully requested that the application be reconsidered, that claims 1-8 be allowed, and that the application be passed to issue.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

A provisional petition is hereby made for any extension of time necessary for the continued pendency during the life of this application. Please charge any fees for such provisional petition and any deficiencies in fees and credit any overpayment of fees for the petition or for entry of this amendment to Attorney's Deposit Account No. 50-2041 (Whitham, Curtis & Christofferson P.C.).

Respectfully submitted,



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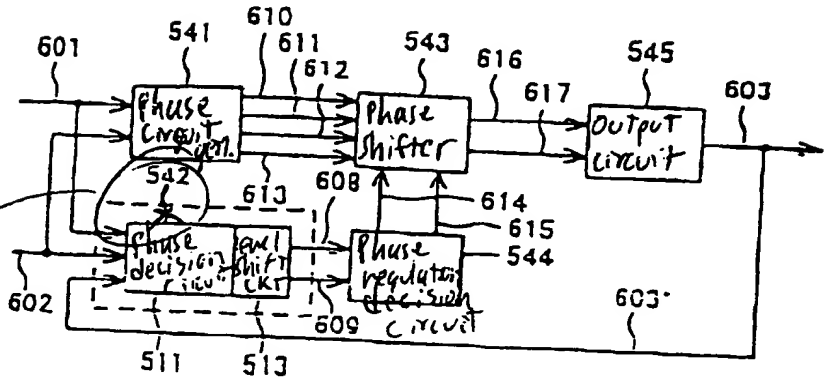
ANNOTATED MARKED-UP DRAWING

FIG. 1 PRIOR ART

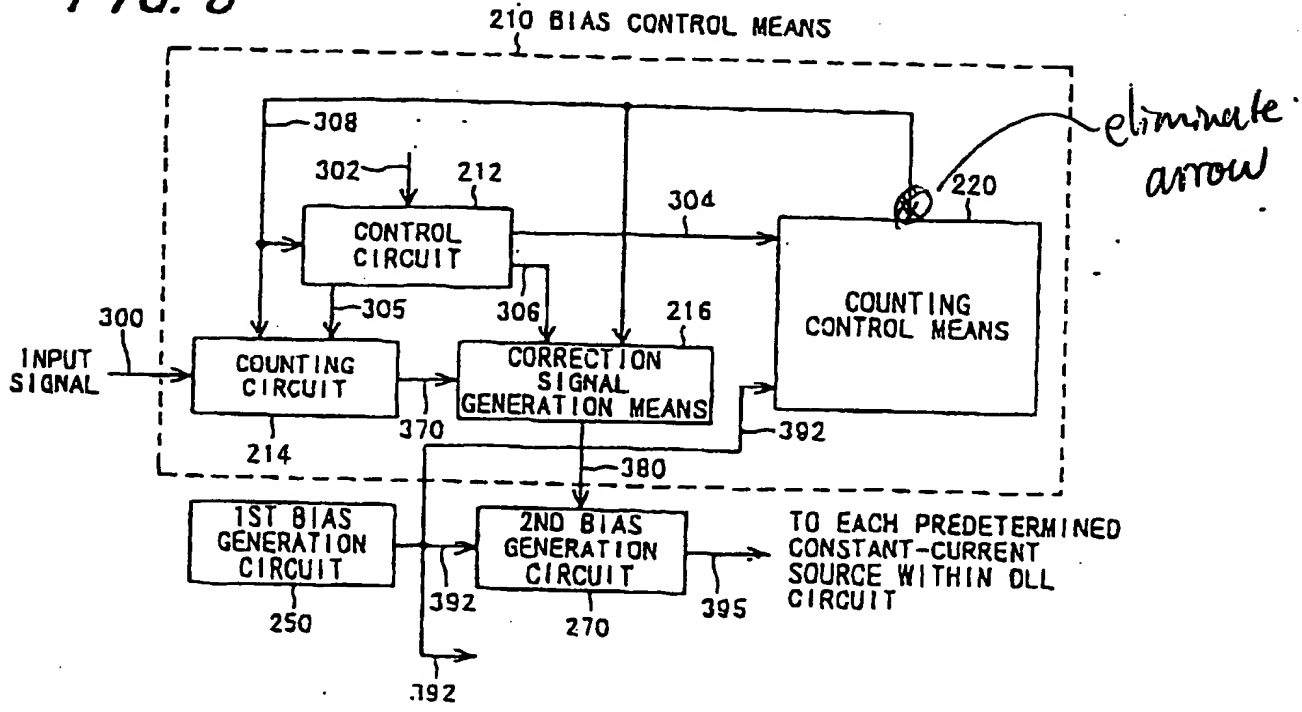


Shorten lead line

enlarge drawing and add labels

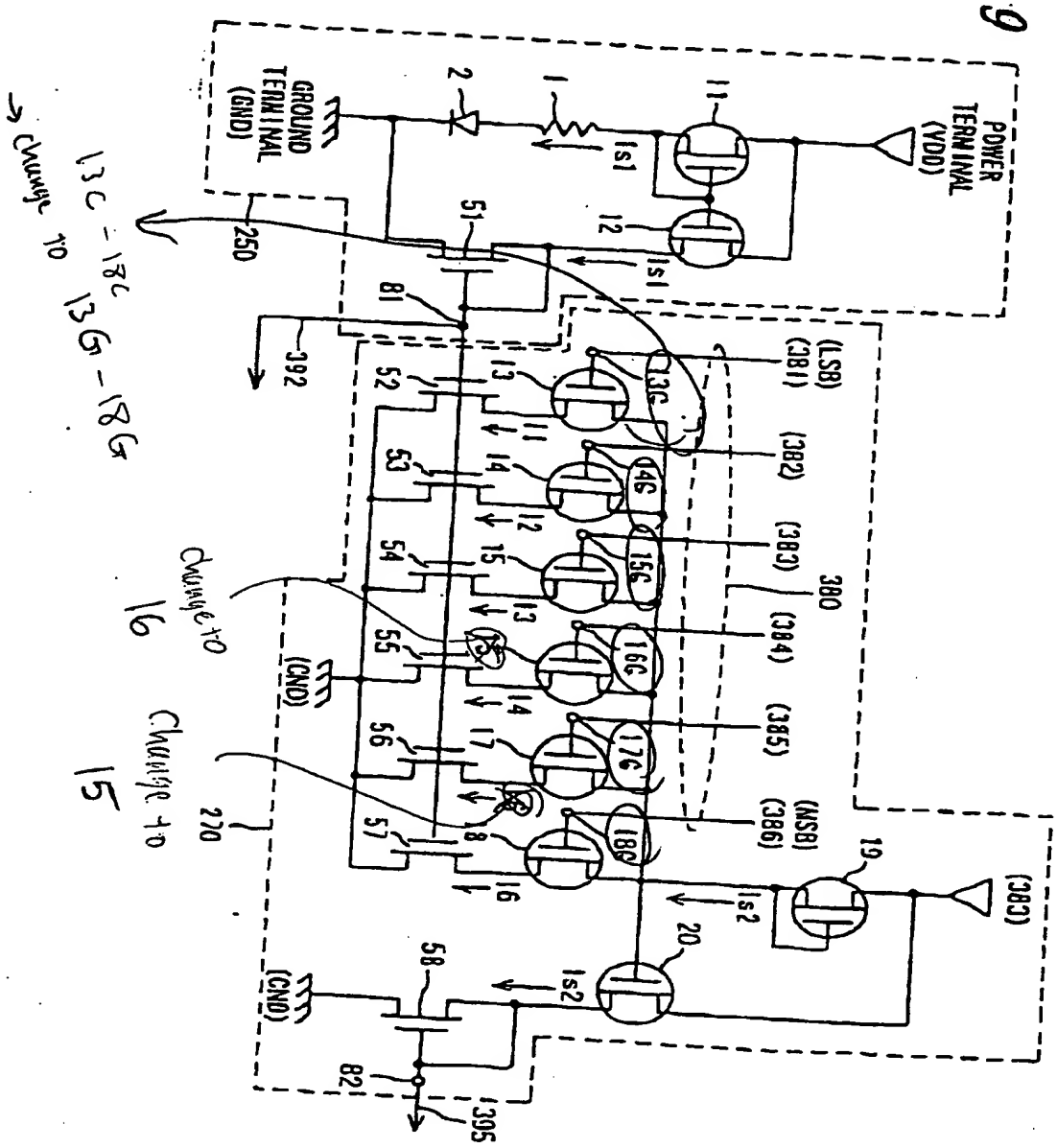
ANNOTATED MARKED-UP DRAWING

FIG. 8



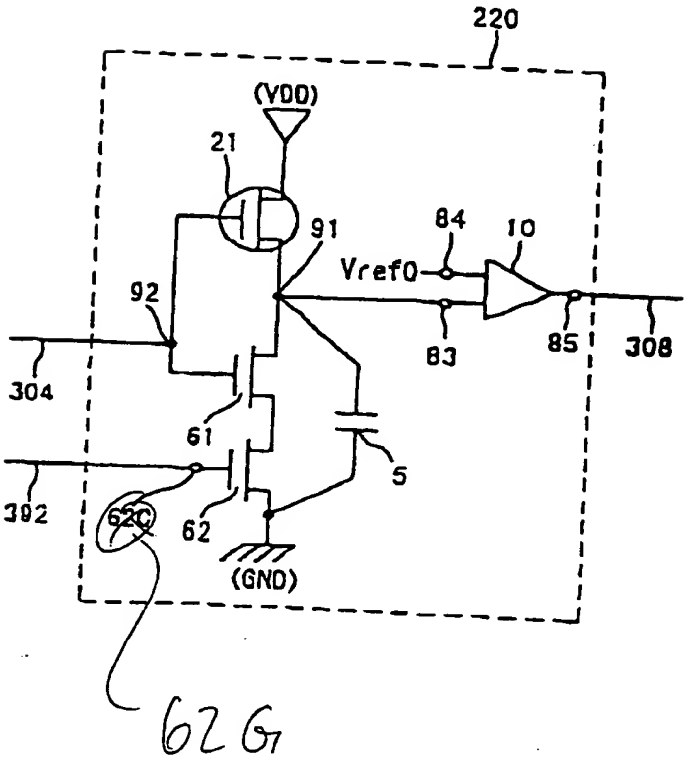
ANNOTATED MARKED-UP DRAWING

FIG. 9



ANNOTATED MARKED-UP
DRAWING

FIG. 10



ANNOTATED MARKED-UP DRAWING

FIG. 11A

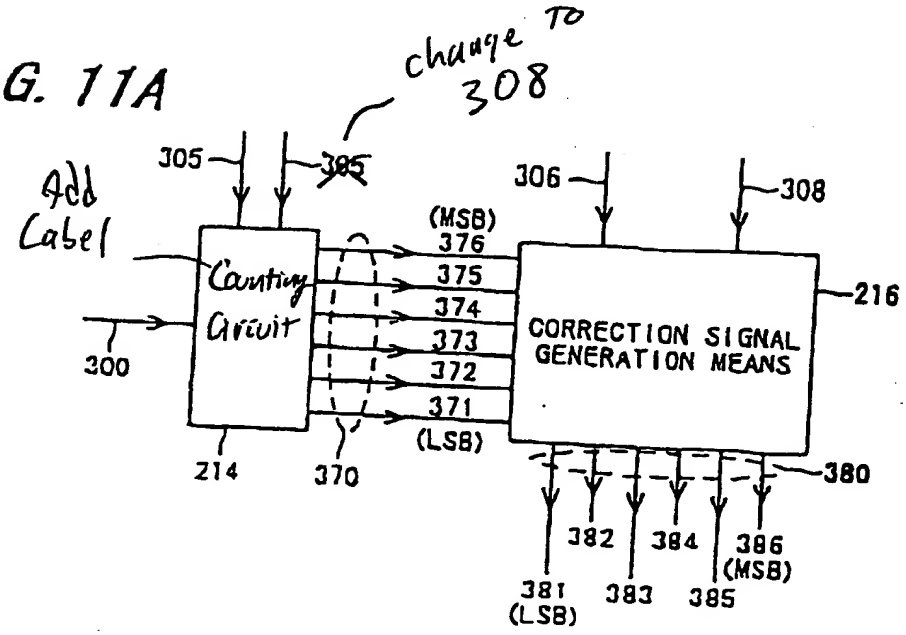
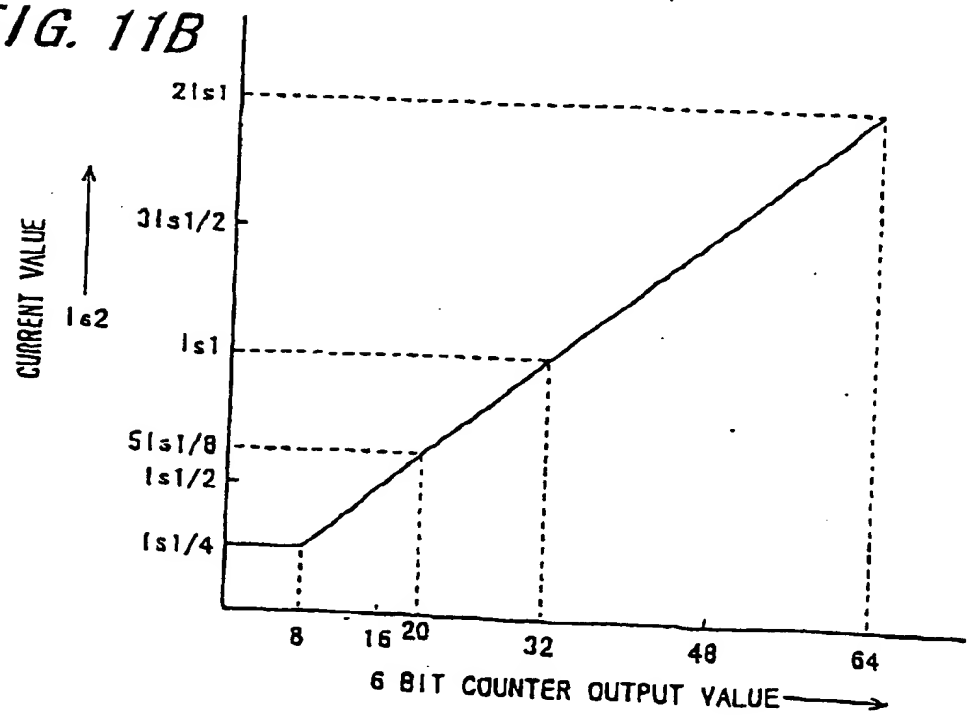
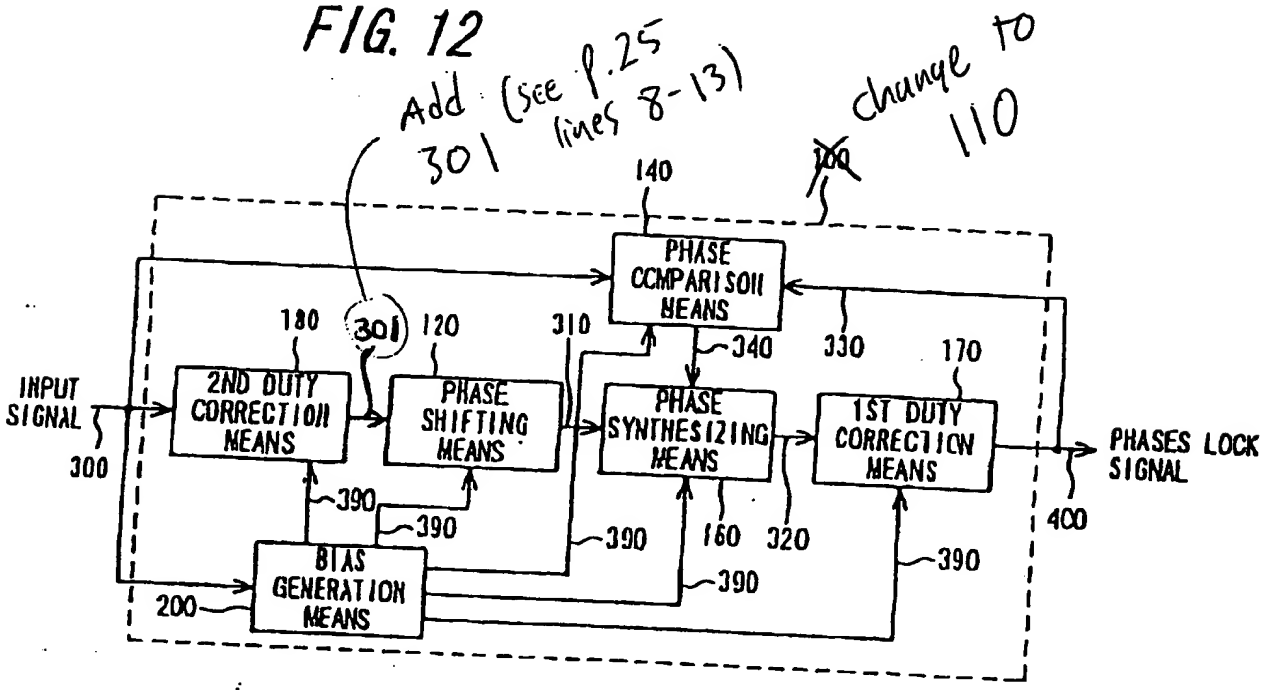


FIG. 11B



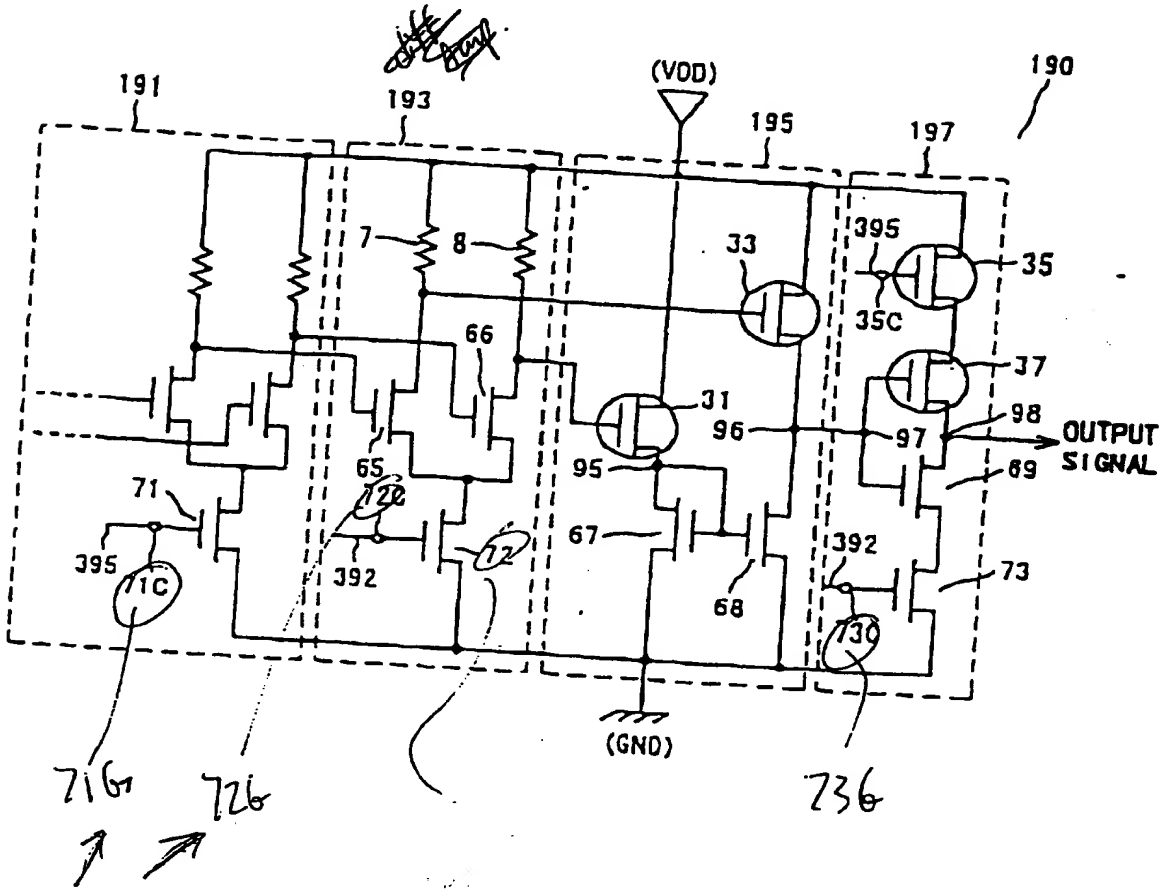
ANNOTATED MARKED-UP DRAWING

FIG. 12



ANNOTATED MARKED-UP DRAWING

FIG. 13



Change "C" to "G"